REMARKS

Introduction

Claims 1-37 are pending in this application.

Applicant has amended claims 1, 9, 20, 24, 28, and 34 to more particularly define the invention. No new matter has been added and the amendments are fully supported and justified by the specification.

Reconsideration of this application in light of the following remarks is hereby respectfully requested.

Summary of the Office Action

Claims 1, 2, 4, 5, 7, 8, 24-26, and 34-36 are rejected under 35 U.S.C. § 102(e) as being anticipated by Panchul et al., U.S. Patent No. 6,226,776 (hereinafter "Panchul").

Claim 20 is rejected under 35 U.S.C. § 102(e) as being anticipated by Killian et al., U.S. Patent No. 6,477,683 (hereinafter "Killian").

Claims 3, 27, and 37 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Panchul.

Claims 6, 9-12, 16-19, and 28-33 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Panchul in view of Killian.

Claims 13-15, and 21-23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Panchul in view of Killian in view of Ashar et al., U.S. Patent No. 6,745,160 (hereinafter "Ashar").

Summary of Telephonic Interview

The Examiner, applicant, and applicant's representatives conducted a telephonic interview on September 12, 2005. Applicant and applicant's representatives (i.e., the undersigned agent and Alexander Shvarts, Reg. No. 47,943) wish to thank the Examiner for the courtesies extended during the interview. During the telephonic interview, the Examiner clarified the objections made and positions taken in the Office Action. Applicants' representatives and the Examiner also discussed potential amendments that could be made to the claims to further define the invention.

Applicant's Reply to the Rejection of Claims 1, 24, and 34 under 35 U.S.C. § 102(e)

The Examiner rejected claim 1, 24, and 34 under 35 U.S.C. § 102(e) as being anticipated by Panchul. The Examiner's rejections are respectfully traversed.

Applicant's invention, as defined by amended independent claim 1, is directed toward a method for generating hardware configuration data for a programmable logic resource from software constructs. High-level software programming code, transparent with regard to hardware resources and hardware configuration, is parsed and hardware configuration data is compiled directly from the high-level software programming code. The hardware configuration data would be used to directly configure the programmable logic resource.

Panchul refers to a computer aided hardware design system for converting a high-level programming language, such as ANSI C, into a register transfer level hardware description language (HDL). The high-level programming language, once converted into HDL, can be simulated and synthesized into a gate-level hardware representation.

In response the applicant's reply to the previous Office Action mailed November 13, 2004, the Examiner asserts that the conversion of high-level programming language into HDL referred to by Panchul is equivalent to converting the high-level programming language into "hardware configuration data" as required by applicant's independent claim 1. More particularly, the Examiner asserts that applicant's claimed

hardware configuration data "does not enforce hardware per se nor does it preclude a HDL being compiled into some more concrete entities." Office Action, page 12.

While applicants disagree with the Examiner's assertion, applicant has amended independent claim 1 in order to advance prosecution. Applicant's amended independent claim 1 more clearly specifies that the hardware configuration data compiled directly from the high-level software programming code is directly used to configure a programmable logic resource. In contrast to applicant's amended independent claim 1, the HDL code of Panchul cannot directly configure a programmable logic resource because HDL code must be further synthesized in order to generate hardware representations. Thus, Panchul does not disclose all of the elements of amended independent claim 1.

Accordingly, for at least the above reason, applicant's amended independent claim 1 is allowable over Panchul. Applicant respectfully requests that the rejection of amended independent claim 1 be withdrawn.

Applicant's amended independent claims 24 and 34 are also allowable over Panchul for at least the same reason at applicant's amended independent claim 1. Accordingly,

applicant respectfully requests that the rejection of amended independent claims 24 and 34 be withdrawn.

Applicant's Reply to the Rejection of Claim 20 under 35 U.S.C. § 102(e)

The Examiner rejected claim 20 under 35 U.S.C. § 102(e) as being anticipated by Killian. The Examiner's rejection is respectfully traversed.

Applicant's invention, as defined by amended claim 20, is directed toward a method for optimizing hardware that is generated by a software-to-hardware compiler. During compilation, the software-to-hardware compiler locates at least one expression in a software program that is used more than once and uses a single set of hardware resources to implement the multiple instances of the software expression. Then, during hardware execution run-time, decisions are made whether to use the hardware resources for each instance of the software expression. For example, during compilation a repeatedly used software expression may be implemented using a single shared hardware block (i.e., instead of having a separate hardware block for each instance of the software expression). At hardware execution run-time an arbitrator, for example, can control access to the shared hardware block.

Killian refers to an automated processor design tool. The tool uses a description of a customized processor instruction set to develop an HDL description of the processor. While compiling the processor, the processor's operation can be optimized by searching a program code for multiple instruction patterns that are repeated in the code and replacing the multiple instruction patterns with a single custom instruction. Killian, column 19, lines 35-49.

In response the applicant's reply to the previous Office Action mailed November 13, 2004, in which applicant argued that Killian does not show applicant's claimed feature of selecting at runtime instances that will have access to the single set of hardware resources, the Examiner asserts that:

> The claim does not establish a clear/explicit context that enforces a unique situation in which the step of selecting is necessarily done by a code being executed (i.e., runtime),wherein it is this very code that selects. As recited, no code is being executed and only a method for optimizing is claimed. Office Action, page 13.

While applicants disagree with the Examiner's assertion, applicant has amended independent claim 20 in order to advance prosecution. Applicant's amended independent claim 20 specifies that the selecting of step is performed "during hardware execution run-time." As previously discussed, Killian does not show hardware

instances selected during hardware execution run-time, as required by applicant's amended independent claim 20. Killian merely refers to optimizing software code during compilation. Thus, Killian does not disclose all of the elements of applicant's amended independent clam 20.

Accordingly, for at least the above reason, applicant's amended independent claim 20 is allowable over Killian. Applicant respectfully requests that the rejection of amended independent claim 20 be withdrawn.

Applicant's Reply to the Rejection of
Claims 27 and 37 under 35 U.S.C. § 103(a)

The Examiner rejected claims 27 and 37 under 35 U.S.C. § 103(a) as being obvious over Panchul. The Examiner's rejections are respectfully traversed.

Applicant's amended claim 27 is directed toward a method for mapping software construct variables into hardware constructs based on the software constructs. The software constructs are parsed and software construct variables are mapped into a hardware construct. The hardware construct corresponding to the software construct variable contains a set of wires of which one of the wires indicates whether the variable has been computed and the remainder of the wires indicate the value of the variable. Applicant's amended

claim 37 is directed toward a hardware construct implemented in programmable logic in which a software construct variable is mapped in hardware as a set of wires (e.g., as recited in claim 27).

The Examiner asserts that applicant's independent claims 27 and 37 are obvious over Panchul. In particular, the Examiner asserts that Panchul shows applicant's claimed feature of mapping a software variable into wires. The Examiner further takes official notice by asserting that applicant's claimed feature of using one of the set of wires to indicate whether the variable has been computed is a known concept in the art. Applicant respectfully disagrees with the Examiner's assertions.

Applicant respectfully submits that Panchul does not show or suggests applicant's claimed invention. Panchul refers to mapping software variables into hardware registers and hardware memory. Panchul, column 5, lines 46-55. Panchul does not show mapping software variables into a set of wires, as required by applicant's independent claims 27 and 37.

In contrast to Panchul, applicant's invention implements software variables as a set of wires in order to avoid mapping software variables into hardware registers and

hardware memory. For example, as applicant's specification clearly states, "this implementation [of software variables as registers] inherently leads to inefficiencies," and "[i]n order to avoid the use of too many large multiplexers, variables may be implemented in hardware as a set of wires." Applicant's Specification, page 2, lines 23-25, and page 4, lines 8-10. Panchul fails to show or suggest such an improvement over the reliance on registers. The Examiner has also failed to provide any teaching or motivation to modify Panchul in order to show or suggest this improvement.

Further, applicant respectfully submits that the combination of Panchul with the Examiner's official notice (which applicant contests) also fails to show or suggest applicant's claims invention. The Examiner takes official notice that a valid or enable bit was known in the art. However, the general use of an enable bit is not the subject of applicant's independent claims 27 and 37. Accordingly, whether taken alone or in combination with the official notice, Panchul does not show or suggest mapping a software variable into set of wires where one of the wires indicates whether a variable have been computed and the remainder of the wires indicate the value of the variable.

Further, there is no motivation to modify Panchul in the manner suggested by the Examiner. The Examiner asserts that the motivation for this combination comes from the fact that wires transporting data require control and that a control bit or wire would provide this control. Office Action, page 7. However, there are many techniques that may be used to provide this control. Applicant respectfully submits that the Examiner has not provided an objective teaching that would suggest this modification. Rather, applicant submits that with the knowledge of applicant's novel method for representing a software construct variable as a hardware construct, particular techniques in the prior art were identified for use in rejecting applicant's invention. This process has long been held invalid by the courts at creating a *prima facie* case of obviousness. See In re Fine, 5 USPQ2d at 1600. ("One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.").

Without a proper motivation for combining the references, the Examiner has "simply take[n] the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability," a practice that is insufficient as

a matter of law. In re Dembiczak, 175 F.3d 994, 999. In doing so, the Examiner has demonstrated mere hindsight reconstruction, the very "syndrome" that the requirement for objective evidence is designed to combat, and the rejection is therefore insufficient as a matter of law. Id.

Accordingly, for at least the above reasons, applicant's amended independent claims 27 and 37 are allowable over Panchul. Applicant respectfully requests that the rejection of claims 27 and 37 be withdrawn.

Applicant's Reply to the Rejection of
Claims 9 and 28 under 35 U.S.C. § 103(a)

The Examiner rejected claims 9 and 28 under 35 U.S.C. § 103(a) as being obvious over Panchul in view of Killian. The Examiner's rejections are respectfully traversed.

Applicant's invention, as defined by amended independent claims 9 and 28, is directed toward a method and programmable logic resource for exploiting parallelism by making speculation decisions at hardware execution run-time. A control flow is generated in the hardware, in which the control flow indicates the status of a block (e.g., status reflects the block's capability for speculation). At hardware execution run-time, the hardware can make decisions

regarding execution of the block at least partially based on the control flow. For example, hardware control flow is synthesized using a special set of control flow wires that are used to enable or disable operations within blocks. One of the operations enabled by the control flow wires is speculative execution (i.e., the ability to execute a block even though it is not guaranteed that the result will be needed). The control flow values of a block may change during hardware execution run-time to allow speculation.

In response the applicant's reply to the previous Office Action mailed November 13, 2004, the Examiner asserts that applicant's claims do not require that the decisions regarding speculative execution be made during hardware run-time.

While applicant disagrees with the Examiner's assertion, applicant has amended independent claim 20 in order to advance prosecution. Applicant's amended independent claims 9 and 28 specify that the decisions regarding execution of a block is performed "at hardware execution run-time." As previously discussed, any decisions about parallelism made by the system of Panchul occur during compilation into HDL and not at run-time. Applicant has also shown, with respect to applicant's independent claim 20, that

Killian also fails to show making decisions at hardware execution run-time. Thus, whether taken alone or in combination, neither Panchul nor Killian show or suggest making decisions at hardware execution run-time as required by applicant's amended independent claims 9 and 28.

Moreover, there is no motivation to modify Panchul in the manner suggested by the Examiner. The Examiner asserts that it would have been obvious to modify Panchul because "speculative executions can avert data fetching exceptions." Id. Applicant respectfully submit that the Examiner has only alluded to a general benefit of speculation without providing an objective teaching that would provide motivation to modify Panchul to generate hardware that exploits parallelism by making decisions at run-time, as required by applicant's amended claim.

Applicant further submits that with the knowledge of applicant's novel invention, particular techniques in the prior art were identified for use in rejecting applicant's invention. This practice has long been held invalid by the courts at creating a *prima facie* case of obviousness. See In re Fine, at 1600. ("One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.").

Without a proper motivation for combining the references, the Examiner has "simply take[n] the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability," a practice that is insufficient as a matter of law. In re Dembiczak at 999. In doing so, the Examiner has demonstrated mere hindsight reconstruction, the very "syndrome" that the requirement for objective evidence is designed to combat, and the rejection is therefore insufficient as a matter of law. Id.

Accordingly, for at least the above reasons, applicant's amended independent claims 9 and 28 are allowable over Panchul. Applicant respectfully requests that the rejection of claims 9 and 28 be withdrawn.

Applicant's Reply to the Rejection of
Claims 2-8, 10-19, 21-23, 25, 26, 29-33, 35, 36

The Examiner rejected claims 2, 4, 5, 7, and 8 under 35 U.S.C. § 102(e) as being anticipated by Panchul. The Examiner rejected claim 3 under 35 U.S.C. § 103(a) as being unpatentable over Panchul. The Examiner rejected claim 6 under 35 U.S.C. § 103(a) as being unpatentable over Panchul in view of Killian. Claims 2-8 are allowable at least because they depend from allowable independent claim 1.

Applicant respectfully requests that the rejection of claims 2-8 be withdrawn.

The Examiner rejected claims 25, 26, 35, and 36 under 35 U.S.C. § 102(e) as being anticipated by Panchul. Claims 25, 26, 35, and 36 are allowable at least because they depend from allowable independent claims 24 and 34. Applicant respectfully requests that the rejection of claims 25, 26, 35, and 36 be withdrawn.

The Examiner rejected claims 21-23 under 35 U.S.C. § 103(a) as being unpatentable over Panchul in view of Killian in view of Ashar. Claims 21-23 are allowable at least because they depend from allowable independent claim 20. Applicant respectfully requests that the rejection of claims 21-23 be withdrawn.

The Examiner rejected claims 10-19 and 29-33 under 35 U.S.C. § 103(a) as being unpatentable over Panchul in view of Killian. Claims 10-19 and 29-33 are allowable at least because they depend from allowable independent claims 9 and 28. Applicant respectfully requests that the rejection of claims 10-19 and 29-33 be withdrawn.

Conclusion

For at least the foregoing reasons, applicant respectfully submits that this application is in condition for allowance.

Accordingly, prompt reconsideration and allowance of this application are respectfully requested.

Respectfully submitted,

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